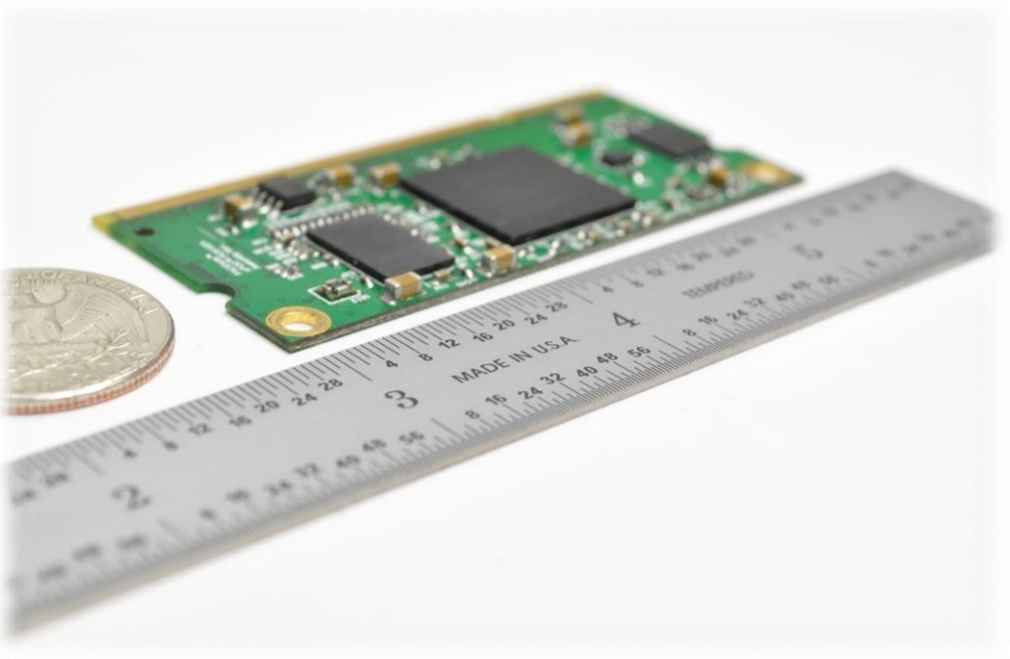
Versachip

xPOD Spartan

Datasheet

May 15, 2013 (v2.1)



Revision history

Version	Date	Description
1.0	10/23/2011	Initial document release
2.0	04/24/2013	Updated to reflect changes in card edge pin assignments as well as new FPGA pin numbers. Added description of the new LEDs interface.
2.1	05/15/2013	Added the mechanical board outline drawing. Refer to Appendix B: Mechanical board outline.

Table of Contents

Overview

The xPOD module XPD104-xx combines low cost Spartan-6 class FPGA technology with basic requirements of today's FPGA based designs such as DDR2 memory, non-volatile configuration storage, clock, and power regulation. Combined with a high density SODIMM interface the xPOD module delivers a complete FPGA solution well suited for new product development, prototyping, or an upgrade for existing system.

Designers now have the option to lay out their main board with an SODIMM connector and "plug in" the FPGA subsystem. BGA package technology, FPGA technology, and DDR2 timing/voltage are all taken care of in one module saving cost, reducing risk, while providing a cost reduction path to tomorrow's FPGA technologies.

xPOD based docking stations are available for rapid development and evaluation.

Features

FPGA	Xilinx Spartan-6 LX45
SODIMM Form Factor	200 Pin High Density Interface
	123 GPIO
	60 differential pairs
	User specified voltage on banks 0 and 1
Volatile RAM	DDR2 memory
	1Gb at 625Mbps
Non-volatile RAM	SPI Flash memory
	128Mb quad mode
Power Regulation	Complete power solution
	In simplest case only 3.3V required
Flexible clocking options	Onboard clock oscillator or/and user provided clock

Part numbers

Part number	Description
XPD104-01	Spartan 6 LX45 FPGA
XPD104-02	Spartan 6 LX25 FPGA
XPD104-03	Spartan 6 LX9 FPGA

Absolute ratings

	Min	Max
Storage temperature	-55C	+125C
Operating temperature	0C	+85C
3.3V power rail	0V	+4V
VCCO_B0, VCCO_B1	-0.6V	+4.1V

Module interfaces

Power

This section describes the xPOD power requirements.

xPOD edge connector allocates ~35% of pins for power and ground. The power pins are split onto three groups: VCC3V3, VCCO_B0, VCCO_B1.

The VCC3V3 pins must be connected to 3.3V rail. This voltage is used to power the onboard active components, power supplies, and bank 2 of the FPGA. The FPGA bank 2 requires 3.3V VCC. The VCC3V3 power rail must be within 10% tolerance range. At power up the voltage must be monotonically rising.

Banks 0 and 1 (VCCO_B0, VCCO_B1 respectively) may be powered with separate voltage rails, or with the same 3.3V rail. In a simple application all banks are powered by the same 3.3V rail.

Bank 3 is used for DDR2 interface and is not available for user I/O.

FPGA

This section provides details to the onboard FPGA.

User IO

xPOD features the Xilinx Spartan 6 FPGA.

There are 123 pins available for user I/O comprised of 60 differential pairs and three unpaired pins. 23 out of 123 user I/O pins are clock enabled pins allowing for external clock inputs (12 diff.pairs + 1 single). Refer to Appendix A: SODIMM Card Edge Pin Assignments for detailed information about the card edge pin assignments.

Dedicated pins

The following table describes the onboard biasing of the FPGA dedicated pins. Description of the purpose and use of the dedicated pins is outside of the scope of this document. Please refer to Xilinx datasheets and user guides listed at the end of this section for more details.

Pin Name	Biasing	Notes
HSWAPEN	None	Controlled by user
DONE	None	Available to user
SUSPEND	None	Controlled by user
INIT	Pull-up to 3.3V (4.7kOhm)	Controlled by user
PROGRAM_B	None	Controlled by user
M0	Pull-up to 3.3V	Not available to user
M1	Pull-down	
TDI	None	Standard JTAG interface. May be daisy-chained with other devices.
TDO	Series 33 Ohm termination	
TCK	None	
TMS	None	

According with biasing of the configuration mode pins M[1:0] FPGA is configures in Master Serial/SPI mode.

For more information about Xilinx Spartan 6 FPGA refer to:

http://www.xilinx.com/products/silicon-devices/fpga/spartan-6/index.htm

DDR2 SDRAM

The xPOD module uses a single 1Gbit DDR2 memory device driven from the integrated memory controller of the Spartan-6 FPGA. The DDR2 device is (or is equivalent to) a Micron MT47H64M16HR-25H providing a 16-bit bus and 64M locations. DDR2 operation up to 312.5 MHz (625Mbps) has been tested on the module. The module supports implementations with and without the internal FPGA termination. Both implementations have been tested at maximum speed. For temperature considerations it is advised to use DDR2 SDRAM interface implementation without the internal termination.

Notes:

- The RZQ pin of the FPGA DDR2 interface is pulled low with 100 Ohm resistor.
- Pins CKE, ODT, and CS of the DDR2 memory are pulled low.

Onboard clock

The xPOD module contains a 40MHz onboard clock source (Kyocera KC3225A-C3 Series). The clock signal is terminated with 33 Ohm resistor. The clock enable signal has a pull-up resistor connected to it. The clock enable signal is connected to FPGA pin U7 and is available to the user.

SPI FLASH

The xPOD module includes 128Mbit SPI Flash device (Micron N25Q128). Module supports single, dual, and quad operations.

The onboard biasing of the SPI NVM pins is as follows:

Pin#	Pin name	Notes
1	Chip select	Pull-up to 3.3V with 4.7 kOhm
2	DQ1	Series termination with 33 Ohm
3	WP/Vpp/DQ2	Series termination with 33 Ohm, pull-up to 3.3V with 4.7 kOhm
4	Vss	Gnd
5	DQ0	Series termination with 33 Ohm
6	SCK	No termination or pull-up/down
7	Hold/DQ3	Series termination with 33 Ohm, pull-up to 3.3V with 4.7 kOhm
8	Vcc	3.3V

JTAG

The xPOD module's JTAG interface has one device (FPGA) in the JTAG chain. The JTAG interface may be daisy-chained with other devices. The JTAG TDO is terminated with 33 Ohm near FPGA. The rest of JTAG pins have no termination as well as no pull-up/down resistors.

LEDs

The xPOD module has two green LEDs available to the user.

The LEDs are connected to FPGA pins U8 and V8. Driving these pins high turns the LEDs on.

Appendix A: SODIMM Card Edge Pin Assignments

Legend		
	GCLK	Clock enabled pin
	_P	Positive side of diff.pair
	_N	Negative side of diff.pair

SO-DIMM pin	LX45-CSG324 pin short name	LX25-LX45-CSG324 pin number	LX45-CSG324 pin full name	LX45-CSG324 Bank number	Notes
1		GND			
2		GND			
3		VCC3V3			
4		VCC3V3			
5	L53_N	N14	IO_L53N_VREF_1	1	
6	L52_P	U17	IO_L52P_M1DQ14_1	1	
7	L53_P	M14	IO_L53P_1	1	
8	L52_N	U18	IO_L52N_M1DQ15_1	1	
9	L50_N	N16	IO_L50N_M1UDQSN_1	1	
10	L51_N	T18	IO_L51N_M1DQ13_1	1	
11	L50_P	N15	IO_L50P_M1UDQS_1	1	
12	L51_P	T17	IO_L51P_M1DQ12_1	1	
13		GND			
14		GND			
15		VCCO_B1			
16		VCCO_B1			
17	L74_P	P15	IO_L74P_AWAKE_1	1	
18	L49_P	P17	IO_L49P_M1DQ10_1	1	
19	L74_N	P16	IO_L74N_DOUT_BUSY_1	1	
20	L49_N	P18	IO_L49N_M1DQ11_1	1	
21	L34_P	K12	IO_L34P_A13_M1WE_1	1	
22	L45_P	K17	IO_L45P_A1_M1LDQS_1	1	
23	L34_N	K13	IO_L34N_A12_M1BA2_1	1	
24	L45_N	K18	IO_L45N_A0_M1LDQSN_1	1	
25		GND			
26		GND			
27	L48_P	N17	IO_L48P_HDC_M1DQ8_1	1	
28	L47_P	M16	IO_L47P_FWE_B_M1DQ0_1	1	
29	L48_N	N18	IO_L48N_M1DQ9_1	1	
30	L47_N	M18	IO_L47N_LDC_M1DQ1_1	1	
31	L40_P	L12	IO_L40P_GCLK11_M1A5_1	1	
32	L46_P	L17	IO_L46P_FCS_B_M1DQ2_1	1	
33	L40_N	L13	IO_L40N_GCLK10_M1A6_1	1	
34	L46_N	L18	IO_L46N_FOE_B_M1DQ3_1	1	
35		GND			

SO-DIMM pin	LX45-CSG324 pin short name	LX25-LX45-CSG324 pin number	LX45-CSG324 pin full name	LX45-CSG324 Bank number	Notes
36		GND			
37		VCCO_B1			
38		VCCO_B1			
39		VCCO_B1			
40		VCCO_B1			
41	L41_N	K16	IO_L41N_GCLK8_M1CASN_1	1	
42	SUSPEND	R16	SUSPEND		
43	L41_P	K15	IO_L41P_GCLK9_IRDY1_M1RASN_1	1	
44	DONE_2	V17	DONE_2	2	
45		GND			
46		GND			
47	L39_P	J13	IO_L39P_M1A3_1	1	
48	L37_P	H15	IO_L37P_A7_M1A0_1	1	
49	L39_N	K14	IO_L39N_M1ODT_1	1	
50	L37_N	H16	IO_L37N_A6_M1A1_1	1	
51		VCC3V3			
52		VCC3V3			
53	L38_P	G16	IO_L38P_A5_M1CLK_1	1	
54	L43_N	H18	IO_L43N_GCLK4_M1DQ5_1	1	
55	L38_N	G18	IO_L38N_A4_M1CLKN_1	1	
56	L43_P	H17	IO_L43P_GCLK5_M1DQ4_1	1	
57		GND			
58		GND			
59	L35_P	F17	IO_L35P_A11_M1A7_1	1	
60	L42_N	L16	IO_L42N_GCLK6_TRDY1_M1LDM_1	1	
61	L35_N	F18	IO_L35N_A10_M1A2_1	1	
62	L42_P	L15	IO_L42P_GCLK7_M1UDM_1	1	
63		VCC3V3			
64		VCC3V3			
65	L29_P	C17	IO_L29P_A23_M1A13_1	1	
66	L36_P	H13	IO_L36P_A9_M1BA0_1	1	
67	L29_N	C18	IO_L29N_A22_M1A14_1	1	
68	L36_N	H14	IO_L36N_A8_M1BA1_1	1	
69		GND			
70		GND			
71	TMS	B18	TMS		
72	L44_N	J18	IO_L44N_A2_M1DQ7_1	1	
73	TDO	D16	TDO		
74	L44_P	J16	IO_L44P_A3_M1DQ6_1	1	
75		GND			
76		GND			
77	TDI	D15	TDI		
78	L30_N	G14	IO_L30N_A20_M1A11_1	1	

SO-DIMM pin	LX45-CSG324 pin short name	LX25-LX45-CSG324 pin number	LX45-CSG324 pin full name	LX45-CSG324 Bank number	Notes
79	L32_N	G13	IO_L32N_A16_M1A9_1	1	
80	L30_P	F14	IO_L30P_A21_M1RESET_1	1	
81		GND			
82		GND			
83	L33_P	E16	IO_L33P_A15_M1A10_1	1	
84	L31_N	D18	IO_L31N_A18_M1A12_1	1	
85	L33_N	E18	IO_L33N_A14_M1A4_1	1	
86	L31_P	D17	IO_L31P_A19_M1CKE_1	1	
87		GND			
88		GND			
89	TCK	A17	TCK		
90	L32_P	H12	IO_L32P_A17_M1A8_1	1	
91		VCC3V3			
92		VCC3V3			
93	L62_P	B14	IO_L62P_0	0	
94	L1_N	F16	IO_L1N_A24_VREF_1	1	
95	L62_N	A14	IO_L62N_VREF_0	0	
96	L1_P	F15	IO_L1P_A25_1	1	
97		GND			
98		GND			
99	L64_N	A15	IO_L64N_SCP4_0	0	
100	L66_P	B16	IO_L66P_SCP1_0	0	
101	L64_P	C15	IO_L64P_SCP5_0	0	
102	L66_N	A16	IO_L66N_SCP0_0	0	
103		GND			
104		GND			
105	L35_P	B9	IO_L35P_GCLK17_0	0	
106	L65_N	C14	IO_L65N_SCP2_0	0	
107	L35_N	A9	IO_L35N_GCLK16_0	0	
108	L65_P	D14	IO_L65P_SCP3_0	0	
109		VCCO_B0			
110		VCCO_B0			
111		VCCO_B0			
112		GND			
113	L34_P	D9	IO_L34P_GCLK19_0	0	
114	L36_N	C11	IO_L36N_GCLK14_0	0	
115	L34_N	C9	IO_L34N_GCLK18_0	0	
116	L36_P	D11	IO_L36P_GCLK15_0	0	
117		GND			
118		GND			
119	L41_P	B12	IO_L41P_0	0	
120	L63_P	F13	IO_L63P_SCP7_0	0	

SO-DIMM pin	LX45-CSG324 pin short name	LX25-LX45-CSG324 pin number	LX45-CSG324 pin full name	LX45-CSG324 Bank number	Notes
121	L41_N	A12	IO_L41N_0	0	
122	L63_N	E13	IO_L63N_SCP6_0	0	
123		VCC3V3			
124		VCC3V3			
125	L6_N	A5	IO_L6N_0	0	
126	L37_N	A10	IO_L37N_GCLK12_0	0	
127	L6_P	C5	IO_L6P_0	0	
128	L37_P	C10	IO_L37P_GCLK13_0	0	
129		GND			
130		GND			
131	L5_N	A4	IO_L5N_0	0	
132	L39_N	A11	IO_L39N_0	0	
133	L5_P	B4	IO_L5P_0	0	
134	L39_P	B11	IO_L39P_0	0	
135		VCC3V3			
136		VCC3V3			
137	L4_N	A3	IO_L4N_0	0	
138	L38_N	F9	IO_L38N_VREF_0	0	
139	L4_P	B3	IO_L4P_0	0	
140	L38_P	G9	IO_L38P_0	0	
141		GND			
142		GND			
143	L1_N	C4	IO_L1N_VREF_0	0	
144	L1_P	D4	IO_L1P_HSWAPEN_0	0	
145		VCCO_B0			
146		VCCO_B0			
147	L10_P	C7	IO_L10P_0	0	
148	L33_P	B8	IO_L33P_0	0	
149	L10_N	A7	IO_L10N_0	0	
150	L33_N	A8	IO_L33N_0	0	
151		VCC3V3			
152		VCC3V3			
153	L3_N	C6	IO_L3N_0	0	
154	L2_N	A2	IO_L2N_0	0	
155	L3_P	D6	IO_L3P_0	0	
156	L2_P	B2	IO_L2P_0	0	
157		GND			
158		GND			
159	L31_P	R8	IO_L31P_GCLK31_D14_2	2	
160	L49_N	V5	IO_L49N_D4_2	2	
161	L31_N	T8	IO_L31N_GCLK30_D15_2	2	
162	L49_P	U5	IO_L49P_D3_2	2	
163		GND			

SO-DIMM pin	LX45-CSG324 pin short name	LX25-LX45-CSG324 pin number	LX45-CSG324 pin full name	LX45-CSG324 Bank number	Notes
164		GND			
165	L64_P	N5	IO_L64P_D8_2	2	
166	L62_N	T3	IO_L62N_D6_2	2	
167	L64_N	P6	IO_L64N_D9_2	2	
168	L62_P	R3	IO_L62P_D5_2	2	
169		GND			
170		GND			
171	L29_N	T10	IO_L29N_GCLK2_2	2	Not part of diff pair
172	L30_P	U10	IO_L30P_GCLK1_D13_2	2	
173	L13_N	P12	IO_L13N_D10_2	2	Not part of diff pair
174	L30_N	V10	IO_L30N_GCLK0_USERCCLK_2	2	
175	L65_P	U3	IO_L65P_INIT_B_2	2	Not part of diff pair
176	L14_N	V13	IO_L14N_D12_2	2	
177	PROGRAM_B_2	V2	PROGRAM_B_2	2	
178	L14_P	U13	IO_L14P_D11_2	2	
179		VCC3V3			
180		VCC3V3			
181	L63_N	V4	IO_L63N_2	2	
182		VCC3V3			
183	L63_P	T4	IO_L63P_2	2	
184	L48_N	T5	IO_L48N_RDWR_B_VREF_2	2	
185	L32_P	T9	IO_L32P_GCLK29_2	2	
186	L48_P	R5	IO_L48P_D7_2	2	
187	L32_N	V9	IO_L32N_GCLK28_2	2	
188		GND			
189		GND			
190	L2_P	U16	IO_L2P_CMPCLK_2	2	
191	L46_N	T7	IO_L46N_2	2	
192	L2_N	V16	IO_L2N_CMPMOSI_2	2	
193	L46_P	R7	IO_L46P_2	2	
194		GND			
195		GND			
196	L16_N	T11	IO_L16N_VREF_2	2	
197	L23_P	U11	IO_L23P_2	2	
198	L16_P	R11	IO_L16P_2	2	
199	L23_N	V11	IO_L23N_2	2	
200	GND	GND			

Appendix B: Mechanical board outline